Please type a plus sign (+) inside this box → [+]

PTO/SB/05 (1/98)

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 0756-2100

First Inventor or Application Identifier: Hongyong ZHANG et al.

Title: METHOD FOR LASER-PROCESSING SEMICONDUCTOR DEVICE

Express Mail Label No.

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [X] Fee Transmittal Form (e.g., PTO/SB/17)
   (Submit an original, and a duplicate for fee processing)
2. [X] Specification *Total Pages* [27]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) (35 USC 113) *Total Sheets* [9]
4. [X] Oath or Declaration *Total Pages* []
   a. [] Newly executed (original or copy)
   b. [X] Copy from a prior application (37 CFR 1.63(d))
      (for continuation/divisional with Box 17 completed)
      [Note Box 5 below]
      i. [] DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [] Incorporation By Reference *(useable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

ADDRESS TO:

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

6. [] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission
   (if applicable, all necessary)
   a. [] Computer Readable Copy
   b. [] Paper Copy (identical to computer copy)
   c. [] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [] Assignment Papers (cover sheet & document(s))
9. [] 37 CFR 3.73(b) Statement [] Power of Attorney
   (when there is an assignee)
10. [] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement [X] Copies of IDS
    (IDS)/PTO-1449 Citations
12. [X] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503)
    (Should be specifically itemized)
14. [] *Small Entity [] Statement filed in prior application,
    Statement(s) Status still proper and desired
    (PTO/SB/09-12)
15. [] Certified Copy of Priority Document(s)
    (if foreign priority is claimed)
16. [X] Other: Request for Interference

*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.

17. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
[] Continuation [X] Divisional [] Continuation-in-part (CIP) of prior application No. 09/236,620 filed January 26, 1999; which itself is a Divisional of Serial No. 08/641,695 filed May 2, 1996 (now U.S. Patent No. 6,096,581 issued 08/01/00); which is a Continuation of Serial No. 08/400,867 filed March 8, 1995, abandoned
Prior application information: Examiner: H. Nguyen Group/Art Unit: 2812

18. CORRESPONDENCE ADDRESS

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(Insert Customer No. or Attach bar code label here)

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Signature J. L. Costellia Date: 8/7/00

PTO/SB/17 (1/98)
Approved for use through 09/30/2000. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1. These are the fees effective October 1, 1997. Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12.

Complete If Known	
Application Number	
Filing Date	August 7, 2000
First Named Inventor	Hongyong ZHANG et al.
Examiner Name	
Group Art Unit	
TOTAL AMOUNT OF PAYMENT 1,056.00	Attorney Docket Number 0756-2100

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:
   Deposit Account No. 19-2380
   Deposit Account Name: SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, PC

   [X] Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17
   [ ] Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance

2. [X] Payment Enclosed:
   [X] Check [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	690	201	345	Utility filing fee	[690.00]
106	310	206	155	Design filing fee	[ ]
107	480	207	240	Plant filing fee	[ ]
108	690	208	345	Reissue filing fee	[ ]
114	150	214	75	Provisional filing fee	[ ]
				SUBTOTAL (1)	$690.00

2. EXTRA CLAIM FEES

			Extra Claims		Fee from Below		Fee Paid
Total Claims	36	- 20** =	16	X	18	=	288.00
Independent Claims	4	- 3** =	1	X	78	=	78.00
Multiple Dependent Claims						=	

**or number previously paid, if greater, For Reissues, see below

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple dependent claim
109	78	209	39	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) -366.00 -

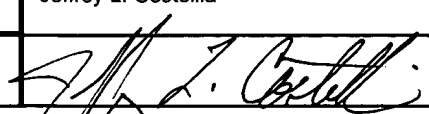
FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge-late filing fee or oath	
127	50	227	25	Surcharge-late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Ext for reply within first month	
116	380	216	190	Ext for reply within second mth	
117	870	217	435	Ext for reply within third mth	
118	1,360	218	680	Ext for reply within fourth mth	
128	1,850	228	925	Ext for reply within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing brief in support of appeal	
121	260	221	130	Request for Oral Hearing	
138	1,510	138	1,510	Petition to institute public use proceeding	
140	110	240	55	Petition to revive-unavoidable	
141	1,210	241	605	Petition to revive-unintentional	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of IDS	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	690	246	345	Filing a submission after final rejection (37 CFR 1.129(a))	
149	690	249	345	For each additional invention to be examined (37 CFR 1.129(b))	
				Other	
				Other	
				*Reduced by Basic Filing Fee Paid	
				SUBTOTAL (3)	$

SUBMITTED BY

Complete (if applicable)

Typed or Printed Name	Jeffrey L. Costellia			Reg. Number	35,483
Signature		Date	08/07/00	Deposit Account User ID	19-2380

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Divisional of U.S. Patent Application No.09/236,620
Attorney Docket No. 0756-2100

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	)	Group Art Unit: not assigned
	)	
Hongyong ZHANG et al.	)	Examiner: not assigned
	)	
Serial No.: Divisional of U.S. Patent Application Serial No. 09/236,620	)	
	)	
Filed: August 7, 2000	)	
	)	
For: METHOD FOR LASER-PROCESSING SEMICONDUCTOR DEVICE	)	

REQUEST FOR INTERFERENCE UNDER 37 C.F.R. §1.607

Assistant Commissioner for Patents
Washington, D. C. 20231

Sir:

Applicants hereby request to have an interference declared between the present application and U.S. Patent No. 5,943,593. Applicants hereby propose a single count as follows:

A method for fabricating a semiconductor device having at least one thin film transistor comprising a channel region and a gate electrode, comprising the steps of:

forming a semiconductor film comprising an amorphous silicon over a substrate; and

irradiating said semiconductor film with a laser light having a rectangular irradiation area while relatively moving said laser light along a scan direction,

wherein said scan direction is parallel to said channel region.

The count is a copy of claim 1 in the present application. Claims 1-14, 16-25 and 27-36 of the present application correspond to the proposed count. Claims 15 and 26 of the present invention application do not correspond to the proposed count. Claims 31-36 of the present application correspond exactly to claims 1-3 and 5-7, respectively, of U.S. Patent No. 5,943,593. Claims 1-8 of U.S. Patent No. 5,943,593 correspond to the proposed count.

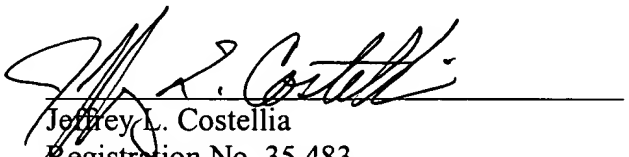
Applicants' application is entitled to priority based on Japanese Patent Application No. 6-665952 filed March 9, 1994 and Japanese Patent Application No. 6-124172 filed May 13, 1994. Thus, Applicants' application predates the earliest priority date of November 10, 1995 for the '593 patent.

Applicants have attached a claim chart indicating where support may be found in the present application for the currently pending claims.

Applicants respectfully request that the Examiner declare an interference between the present application and U.S. Patent No. 5,943,593. Should the Examiner believe that anything further is desirable in order to place the application into better condition for interference the Examiner invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

NIXON PEABODY LLP



Jeffrey L. Costellia
Registration No. 35,483

Attached: Claim Chart

JLC:JEH/dkt
Attorney Docket No.: 0756-2100

NIXON PEABODY LLP
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McLean, Virginia 22102
Telephone (703) 790-9110

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PATENT CLAIMS	SUPPORT IN APPLICATION FOR COPIED CLAIMS
1. A method for fabricating a semiconductor device having at least one thin film transistor comprising a channel region and a gate electrode, comprising the steps of:	
forming a semiconductor film comprising an amorphous silicon over a substrate; and	Page 9, lines 10-11.
irradiating said semiconductor film with a laser light having a rectangular irradiation area while relatively moving said laser light along a scan direction,	Page 7, lines 23-27; Page 10, lines 7-25 and Figs. 2B and 2D.
wherein said scan direction is parallel to said channel region.	Page 10, lines 7-25 and Figs. 2B and 2D.
2. The method of claim 1, wherein said laser light is irradiated from an upper side of said gate electrode.	Page 9, lines 10-27; Page 19, lines 3-6 and Fig. 10E.
3. The method of claim 1, further comprising a step of heating said semiconductor film.	Page 9, lines 15-17.
4. The method of claim 3, wherein said semiconductor film further comprises a metal.	Page 9, lines 12-14.
5. The method of claim 1, wherein said thin film transistor is a top-gate type thin film transistor.	Page 9, lines 10-29.
6. The method of claim 1, wherein said laser light is a pulsed excimer laser.	Page 10, lines 10-17.
7. The method of claim 6, wherein said step of irradiating comprises pulsing said excimer laser ten times.	Page 10, lines 15-17.
8. The method of claim 1, wherein said thin film transistor is used as one of a column driver and a scan driver.	Page 9, lines 32 - Page 10, line 3.

9. The method of claim 1, further comprising the step of introducing a dopant impurity to said semiconductor film before said irradiating step.	Page 9, lines 24-27.
10 A method for fabricating a thin film transistor device having a polycrystalline semiconductor thin film to form a channel region, and a gate electrode which intersects the channel region, comprising the steps of:	
providing a structure comprising a semiconductor thin film separated by a gate insulating layer from a gate electrode on an insulating substrate; and	Page 9, lines 10-23.
irradiating the semiconductor thin film with a laser light having a rectangular irradiation area while relatively moving said laser light along a scan direction which is parallel to the channel region.	Page 10, lines 7-25 and Figs. 2B and 2D.
11. The method of claim 10, wherein said gate electrode is irradiated on an upper side.	Page 9, lines 10-27; Page 19, lines 3-6 and Fig. 10E.
12. The method of claim 10, wherein said irradiating step comprises moving the laser light.	Page 10, lines 7-15.
13. The method of claim 10, wherein said irradiating step comprises partially overlapping irradiation of the laser light.	Page 10, lines 10-17.
14. The method of claim 10, further comprising the step of heating said semiconductor thin film.	Page 9, lines 15-17.
15. The method of claim 14, wherein said semiconductor thin film comprises a metal.	Page 9, lines 12-14.
16. The method of claim 10, wherein said thin film transistor is top-gate type thin film transistor.	Page 9, lines 10-29.
17. The method of claim 10, wherein said laser light is a pulsed excimer laser.	Page 10, lines 10-17.
18 The method of claim 17, wherein said step of irradiating comprises pulsing said excimer laser ten times.	Page 10, lines 15-17.

19. The method of claim 10, wherein said thin film transistor is used as one of a column driver and a scan driver.	Page 9, line 32 - Page 10, line 3.
20. The method of claim 10, further comprising the step introducing a dopant impurity to said semiconductor thin film before said irradiating step.	Page 9, lines 24-27.
21. A method for fabricating a thin film transistor device having a polycrystalline semiconductor thin film to form a channel region, and a gate electrode which intersects the channel region, comprising the steps of:	
providing a structure comprising a semiconductor thin film separated by a gate insulating layer from a gate electrode on an insulating substrate;	Page 9, lines 10-23.
introducing a dopant impurity to said semiconductor thin film; and	Page 9, lines 24-27.
irradiating the semiconductor thin film with a laser light having a rectangular irradiation area while relatively moving said laser light along a scan direction which is parallel to the channel region in order to activate said dopant impurity.	Page 7, lines 23-27; Page 10, lines 17-25 and Figs. 2B and 2D.
22. The method of claim 21, wherein said gate electrode is irradiated on an upper side.	Page 9, lines 10-27; Page 19, lines 3-6 and Fig. 10E.
23. The method of claim 21, wherein said irradiating step comprises moving the laser light.	Page 10, lines 7-15.
24. The method of claim 21, wherein said irradiating step comprises partially overlapping the laser light.	Page 10, lines 10-17.
25. The method of claim 21, further comprising the step of heating said semiconductor thin film.	Page 9, lines 15-17.
26. The method of claim 25, wherein said semiconductor thin film comprises a metal.	Page 9, lines 12-14.

27. The method of claim 21, wherein said thin film transistor is a top-gate type thin film transistor.	Page 9, lines 10-29.
28. The method of claim 21, wherein said laser light is pulsed excimer laser.	Page 10, lines 10-17.
29. The method of claim 28, wherein said step of irradiating comprises pulsing said excimer laser ten times.	Page 10, lines 15-17.
30. The method of claim 21, wherein said thin film transistor is used as one of a column driver and a scan driver.	Page 9, line 32 - Page 10, line 3.
31. A method for fabricating a thin film transistor device having a polycrystalline semiconductor thin film to form a channel region, and a gate electrode which intersects the channel region, comprising the steps of:	
forming a structure comprising an amorphous semiconductor thin film separated by a gate insulating layer from a gate electrode on an insulating substrate; and	Page 9, lines 10-23.
irradiating the amorphous semiconductor thin film with an energy beam having a rectangular irradiation area to convert the amorphous semiconductor thin film into a polycrystalline semiconductor thin film while relatively moving said energy beam along a scan direction which is orthogonal to the gate electrode and is parallel to the channel region.	Page 7, lines 23-37; Page 10, lines 7-25 and Figs. 2B and 2D.
32. A method according to claim 31, wherein said irradiation step is a process for irradiating an amorphous semiconductor thin film to form a polycrystalline semiconductor thin film of the thin film transistor connected to a pixel electrode formed on the insulating substrate.	Page 9, line 33 - Page 10, line 13; Page 19, lines 29-30.

33. A method according to claim 31, wherein said irradiation step is a process for irradiating an amorphous semiconductor thin film to form a polycrystalline semiconductor thin film of the thin film transistor comprised of peripheral driving circuit for an active matrix array.	Page 9, line 33 - Page 10, line 13; Page 19, lines 29-30.
34. A method according to claim 31, wherein said irradiation step is performed by moving the energy beam.	Page 10, lines 7-15.
35. A method according to 31, wherein said irradiation step is performed by partially overlapping irradiation of energy beam.	Page 10, lines 10-17.
36. A method according to claim 31, further comprising steps of forming source and drain regions which comprise doping an impurity to the polycrystalline semiconductor thin film and activating the doped impurity by irradiating an energy beam.	Page 9, lines 24-27.